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CHEETAH

Cost-reduction through material optimisation and Higher EnErgy outpuT of solAr pHotovoltaic modules - joining Europe's Research and Development efforts in support of its PV industry

Deliverable

D5.3 – Mid-term report on the R&D impact on cost reduction

WP5 – Acceleration of innovations' implementation

Section 1 – Document Status

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Section 2 – Table of content

Section 3 – Acknowledgements

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This mid-term report reflects one of the main work-streams of the Cheetah project which is related with the cost assessment of the innovations and the main objectives set by the research partners. Therefore the active participation of the above-mentioned leading institutes was crucial to the development of credible results.

Section 4 – Executive summary

Description of the deliverable content and purpose

With more than 95 GW installed capacity end of 2015, solar photovoltaic (PV) continues being one of the predominant renewable technologies and one of the most promising technologies for Europe to meet its future energy and climate objectives. However, attached to the market growth, the price erosion seen especially over the last five years has created high pressure throughout the whole PV value chain and an uncertain environment for healthy margins. Either due to overcapacity phenomena in the past or due to radical changes of the regulatory framework, prices have always been a matter of high attention.

In a field of increased competition, the cost of PV electricity needs to be further reduced to enable truly large-scale application of photovoltaics in Europe. The rapid price decline of PV systems by more than a factor two in the last three years has already allowed to achieve grid parity for residential applications in several European countries such as Italy, Spain, Germany and The Netherlands. However, further cost reduction is required and this can be achieved also through reduction of (costs of) materials used in PV systems and components, and through improvements in the overall performance of PV systems.

The Cheetah project acknowledging the necessity for further cost reduction but also enhanced performance, aims at developing technologies that use less and more environmental friendly materials and improving the reliability and lifetime of the final product based on high-throughput processes. More specifically and in support of the objectives of the European Energy Research Alliance and the Joint Programme on Photovoltaic Solar Energy (EERA-PV), the project is working among others on high-level technology development in the field of ultra-thin crystalline silicon (c-Si) solar cells and advanced processing steps.

This mid-term report provides a solid estimate mainly from the research community on the cost impact that these technologies could have in comparison with the existing "conventional" c-Si technologies that enjoy the largest share of the PV market (>90%)[1]. A technical innovation attached to a cost impact assessment will give a good understanding on the benefits of those research activities and will potentially accelerate the exploitation by the PV industry. Ultimately such results, even if they are subject for further investigations and validations from the industry, will support relevant discussions on research and funding priorities in Europe and the PV sector.

The current report focuses only on the wafer-based c-Si PV technologies globally assessing the Cheetah research work on ultrathin and epitaxial wafer cells and modules. The report shows that there is a significant potential for further cost reduction that can reach 23,4% on module level when comparing the use of the epitaxial foils developed within the Cheetah project with the use of regular wire-sawn wafers, applying the same chosen benchmark technology for back contact (SHJ-IBC) modules on both types of silicon material.

A future version (final report, end of 2017) will refine the findings of this report by including the effect on the cost of additional Cheetah developments related to cell and module processing of epi-foils and will also include the assessment of the research work on advanced light management for thin-film PV (TF) and on Organic PV (OPV) in accordance with the EERA-PV objectives.

Those two reports together with two background and more fundamental reports – *Analysis of the cost reduction potential of the PV technology (D5.2)* that was produced during the second half of 2015 and

[1] Source: NPD Solabuzz, published by pv-magazine

Benchmark knowledge of the quality and reliability of PV technology (D5.5.) that is expected during Q1 2016 – complete the cost assessment tasks providing a credible analysis and useful both for the research and the industry community to build on.

Section 5 – Deliverable report

1. Introduction

1.1. Rationale

As the sector continuously matures and the competitiveness of the PV technology evolves, new innovative business models emerge that base their success on the true potential of the PV technology and value the performance of the PV system. Therefore, it is very important to investigate and properly assess the future innovations and technology breakthroughs understanding the impact of R&D on the performance, the cost reduction and consequently the PV business. Taking into consideration the future renewable targets (27% of RES by 2030 which also means 45% of RES power) and the important role of PV, it is necessary to foresee its potential and its limitations and draft of a roadmap (also technological) that will allow PV to develop within a focused, sustainable and healthy environment and become a mainstream source of electricity.

Cheetah stands in favour of these objectives for a thorough assessment – not only technical but also economical – that will enable the European research and subsequently industry community to facelift, upscale manufacturing and support the future EU energy targets. Indirectly this will also support additional macroeconomic challenges that Europe is facing. Solar PV has been proved to be a significant component for creating employment and value for Europe[2].

Thanks to its broad consortium and the consolidation of high level of expertise in the PV sector, the CHEETAH project offers a unique opportunity to pool experience and conduct such analysis the results of which will develop an interface between the PV industry and the project incorporating industry's feedback and address challenges. The cost assessment of Cheetah innovations becomes then rather important for all stakeholders and target groups - researchers, industry but also investors.

1.2. Objectives

Taking into consideration the importance of this work but also the limitations within the project the main objective for this mid-term study is to give an updated and solid set of information regarding the potential cost of the suggested ultra-thin wafer based c-Si. The information will of course clarify if the suggested innovations lead to a reduced cost for the final product (cell or/and module) in comparison to the existing "standard" c-Si technologies and also is the magnitude of this reduction. This will set the confidence levels of the actual cost reduction since there are a number of uncertainties and assumptions for this analysis due to current absence of commercial players and proper benchmarking.

The results of this analysis will be subject to comments and possible adaptations upon discussion with external experts and industry representatives. Final cost assessment results will be presented in the final report (end of 2017).

[2] Source: Ernst & Young, October 2015, *"Solar Photovoltaics Jobs & Value Added in Europe"*, published by SolarPower Europe

1.2.1. Cheetah innovations under assessment (mid-term)

The mid-term assessment includes the innovations on the c-Si cluster and in particular covers the ***ultra-thin wafer based cells/modules*** and the **epitaxial wafer (epi-wafer) based cells/modules**. Those innovations are in accordance with the objective of using less material and increasing the performance (power).

- **The Ultra-thin wafer** based product incorporates all the innovations from the Cheetah project that overcome the current bottlenecks for wire-sawn wafers (e.g. wafer breakage, cell processing etc.) and allows the development of a c-Si wafer of 80 µm (with wire sawing), the cell processing of this ultra-thin wafer and the module development with the use of those cells. The current commercial wafers have a thickness of 160 µm to 180 µm (reference). Therefore an intermediate step/product of a wafer 120 µm is also considered in the assessment, which is in industrial predevelopment phase.
- **The Epi-wafer** based product incorporates all the innovations from the Cheetah project that allow the development of a high-quality c-Si thin foil of 40 µm by chemical vapour deposition (CVD) avoiding the wire-sawing process and related kerf losses and drastically shortcutting the value chain of wafer production by avoiding polysilicon formation, ingot formation and wafering.

Both abovementioned innovations reduce the silicon material use and the kerf loss (in wire sawing) - which is on average around 140 µm - along with a reduction of energy and other consumables required for the crystallization and the wafering process. Consequently this could lead to a significant cost reduction.

The innovations under assessment are in line with the objectives of the project and in accordance to the workplan.

1.3. Limitations

This analysis is based on literature review (current relevant publications), own assumptions (knowledge and experience from the research partners) and results extracted by calculation sheets and models built by different project partners. The innovations suggested by Cheetah are still of low readiness level (TRL) and not ready for large scale commercialization which is indeed the ultimate goal in the medium to long run.

Therefore, there are many factors and components that are still unclear and will be subject to supply chain logistics and other macroeconomic factors such as global economic environment, EU competitiveness etc. In addition, standardization around materials and also processes and equipment for these innovations require updates and improvements that will match with the specifications of those new products. This will substantially impact the cost and quality of those products.

In order to overcome some of the abovementioned global limitations, industry involvement at early stages is important and planned with Cheetah. Industry experts with a clearer idea on market boundaries, technical bottlenecks and supply chain management (SCM) challenges will be able to provide a valuable feedback for our cost assessment work. In a volatile market environment as is the case for PV, discussions should continue beyond the duration of the project to ensure an effective implementation of Cheetah innovations.

2. Methodology

As mentioned before the approach that was used for our first cost assessment results was threefold:

- **Literature review:** A sufficiently thorough literature review was conducted in order to mainly retrieve updated information on costs (wafer costs) and efficiencies of different thickness, cell processing and module production costs. The materials reviewed were scientific papers, studies, online information platforms (e.g. **PVinsights**) and relevant articles in international media.
- **Cheetah experts' experience:** The information acquired by the literature review was filtered by the relevant consortium experts and enhanced by own in-house knowledge. Besides the core expert group that actively worked on this mid-term report, the whole consortium (34 research partners) validated the results.
- **Modelling results:** In order to fill in the gap of available information upon the literature review and also to increase the quality of our results, specific partners made use of their own models and calculation sheets to extract results. This was particularly important for the epi-wafer technologies since the available information is limited.
- **Reference and benchmark technologies:** As a first point of reference to assess the Cheetah innovations, the commercially available c-Si module should be taken into consideration. However from a technological perspective the state of the art back contact technology (not yet commercial) is a more logical choice to compare all developments to. Application of the common practice in module assembly to thin cells (tabbing and stringing) will be unlikely. For that reason back contact technology has been appointed the module technology of choice for the project and a silicon heterojunction (IBC-SHJ) concept as described in the article by [Louwen 2016][5] has been chosen as the benchmark technology. With respect to overall module manufacturing costs this benchmark is with estimated 0.51 USD/Wp very close to 0.50 USD/Wp for commercial modules, according to the same article.

2.1. Description of epi-wafer cost calculation model

For the calculation of the cost of an epi-wafer, it was considered that the process for making such a wafer consists of the following steps:

- Reclaim/clean of the parent wafer where the epitaxial Si foil will be grown
- Anodization
- Low hydrogen annealing (H2 anneal) and epitaxial deposition
- Lasering
- Detachment

After which the parent wafer is re-inserted into the first process step until the end of its lifetime. In setting up the cost-calculations, existing data for similar process steps were used as reference. Below, more details are given for each process step. As for the impact of the parent wafer itself on the cost structure of the epi-wafer, a detailed description is given below as well.

Base data

In IMEC's model a depreciation of equipment cost over 7 years is assumed. The model is basically independent of the throughput, but for the calculations a throughput of 3000 wafers/h is assumed. The mechanical yield is taken to be high at 99.8% (see comments on the parent wafer below). Different scenarios have been evaluated with wafer dimensions of 125mm and 156mm although results are presented for 156mm size. All equipment and consumption costs are taken to be independent of wafer size, except for the trichlorosilane (TCS) consumption that is used as precursor, the parent wafer cost and the polysilicon-resale (see below).

Parent wafer

For the parent wafer it is assumed that the cost will follow the same trend as anticipated for thin wafers in [Goodrich 2013][3]. This means that, while cost increases with increased poly-silicon consumption, there will also be cost reductions due to kerf loss recycling, diamond wire usage etc. The parent wafer will be used a number of times, depending on the reclaim procedure and the capability to reliably handle thinned-down wafers. In this way, the cost of the (expensive) parent wafer is distributed over several foils. At the end of its lifetime, the parent will be sold at the actual poly-silicon stock price. The breakage rate of the parent wafers should be relatively low due to the mechanical robustness; however any breakage would result in loss of poly-silicon resale and increased parent wafer consumption.

Reclaim/clean

It is assumed that a similar equipment and consumption cost applies as for a texturing wet bench.

Anodization

A similar equipment price as for a commercial plating tool is assumed. For the chemical consumption, a mixture of hydrogen fluoride (HF) and isopropyl alcohol (IPA) is assumed with a maximum bath lifetime which is similar to experimentally observed bath lifetimes.

H2 anneal and epitaxial deposition

The equipment cost for this step is partly based on feedback from consortium partners. Since wafer loading, temperature transients and H2 anneal are independent of the deposited layer thickness, the equipment cost is assumed to only partly scale with layer thickness. The precursor is TCS, and the usage is taken to be 85% efficient.

Lasering

For this step, conventional tools are used.

Detachment

A relatively simple tool employing a vacuum end effector is envisaged. For this reason, the tool cost and the consumption cost are assumed to be similar to a screen printer, with the exception of paste consumption.

[3] Source: Alan Goodrich, Peter Hacke, Qi Wang, Bhushan Sopori, Robert Margolis, Ted L. James, Michael Woodhouse, *"A wafer-based monocrystalline silicon photovoltaics road map: Utilizing known technology improvement opportunities for further reductions in manufacturing costs", January* 2013, published by NREL

2.2. Assumptions

In this analysis it was sensible to consider certain global assumptions – apart from the model specific ones – based on the availability of data, the timeframe and resources within the project, but also the different calculation methods among the partners. The assumptions were necessary to frame the challenge – which is to prove the cost reduction impact and provide more credible results and benchmark. Due to a number of different processes, materials and supply chain changes the cost assessment task is a highly challenging one and will require further investigation. However, this work provides a solid starting point. The next phase of this work will try to reduce the global assumptions and enter into more details reducing the uncertainty of the results.

2.2.1. Global assumptions

Main assumptions considered are:

- The point of reference for our cost comparisons is year 2015 (second half) which is the time that the analysis has been initiated. In order to proceed to a valid comparison and be able to identify the differences in costs between a "standard" product and a product created within Cheetah project, the comparison should be done at a point of time where the conditions will allow to commercialize the Cheetah innovations based on the assumptions unfolded below. At the same point of time the standard product should probably have another cost (cheaper than today). This point of time is what we refer as "ultimate" below and the Cheetah innovations are assessed with respect to this "ultimate" standard as well.
- The analysis considers a "business as usual" case, meaning that to commercialize the cheetah innovations at high production scales it is assumed that all necessary conditions are in place e.g. technical adaptations and new equipment to handle the new thinner products which will keep the cell production yields at high figures. Therefore, the costs for cell processing are assumed rather constant without specific assumptions (e.g. reductions in metallization etc.). Ultimate numbers are only adopted to the cell processing yields.
- Average costs of commercial cut wafer, cell processing and module development from 2015 were used from public available sources. Those are presented in each subchapter below.
- Current costs for ultra-thin wafers assume commercialization under the current conditions. That implies higher costs than in the ultimate future scenario due to shortcomings in equipment manufacturing process.
- The analysis does not consider gross margins per value chain step – apart from minimum required margins. Therefore cost and price in the report have the same meaning. The cost figures represent the so called Cost of Goods Sold (COGS).
- No taxes are included from the assessment of costs.
- For the silicon (Si) material, the cost assessment assumed an evolution based on experience curves from literature. This supported the assumptions for the future wafer costs (see chapter 6 in section 7 below).
- Average quality wafers have been considered in the study. For prime quality wafers, possibly essential to maintain efficiency levels for thin cells, costs for cut wafers could be 30% higher.

- Regarding the wafer technology, the analysis assumes a similar cost between the multi- and mono-crystalline wafers due mainly to demand differences (over-demand for multi-and under-demand for mono-wafers)[4]. Same assumption is made for the n-type and p-type wafers.
- The size of the wafer considered was 156x156 mm in pseudo-square shape. The yield of this process step for cutting wafers is assumed around 95%.
- For processing/cutting the wafers, diamond wire sawing process is considered to be applied.
- The cost reduction of epi-wafer in comparison to the reference cut wafer assumes a production scale of 1 GWp/year.
- For the assessment of the module cost, the back contact (IBC) technology as presented in the paper by [Louwen 2016][5] has been chosen as a benchmark with the given shares of costs in the modules presented therein (e.g. share of wafer, cell processing, other materials etc.). It assumes an IBC 60 cell module of 20.5 % efficiency and power output of around 300 Wp.
- Due to the global supply chain of PV and with different sources of information, costs are presented in dollars. When needed, an average exchange rate used: 1 USD = 0.9 EUR.

2.2.2. Specific assumptions

Some more specific assumptions are:

- The efficiency for thinner cell modules has been adopted according to the thickness – slightly lower for ultra-thin and epi-foil based modules. These are presented below in the results section.
- Following on the second point of the global assumptions the yield of cell production is assumed rather constant in rates close to 99% with a slight additional reduction of 2 and 4% in ultra-thin and epi-foil substrates respectively due to breakage.
- The cell-to-module (CTM) conversion ratio is assumed to be 97.2%, as can be derived for IBC-SHJ from the paper by [Louwen 2016][5], considering both optical and resistive losses from cell to module. This is assumed equal for all wafer thicknesses.
- No extra or more expensive cell processing steps are assumed, just extra losses due to higher breakage rate and lower efficiencies for lower thicknesses are taken into account.

[4] Sources: pv-magazine and EnergyTrend, published at pv-tech

[5] Source: Atse Louwen, Wilfried van Sark, Ruud Schropp, André Faaij, *"A cost roadmap for silicon heterojunction solar cells",* January 2016, published by Elsevier

3. Results

The cost assessment results are presented separately for wafers, cells and modules summarizing the results for both Cheetah innovations – ultra thin wafers and epi-wafers.

3.1. Impact on wafers costs

Table 1 below summarizes the costs of wafers both for today and for a relevant point in time where the Cheetah innovations are assumed to be commercially available (ultimate wafer cost). The ultra-thin and epi-foil wafers are directly compared with the standard product available now. The comparison is obvious for the current status and for the future – considering a relevant reduction for all thicknesses (also the standard one). An intermediate thickness (120 µm) is included.

Currently the costs of wafers (spot price) are around 0.9 USD[6] for p-type wafers. As mentioned in the global assumption chapter above, this assumes that both multi and mono Si wafers and n-type and p-type wafers have the same production cost. The costs in the table include the polysilicon, the electricity, the depreciation, the sawing and other costs and excludes taxes. The current costs of the thin and ultra-thin wafers were estimated based on relevant literature [Goodrich 2013], [Louwen 2016] (see Figure 1) and adapted according to the consortium's experience.

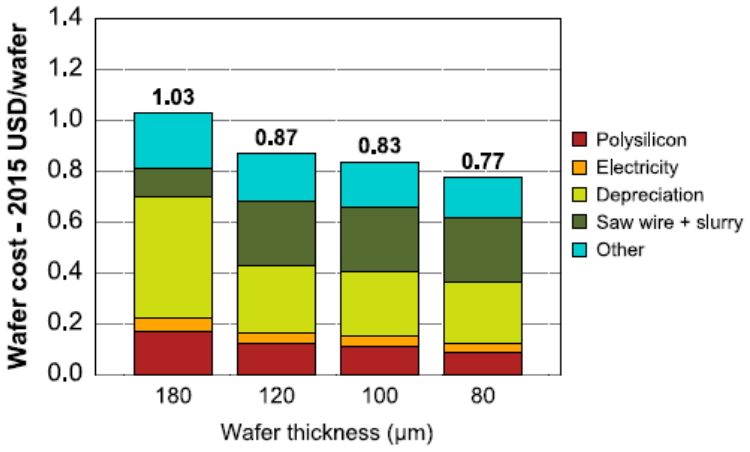

Figure 1: Wafer production costs for various wafer thicknesses. The polysilicon cost is included [Louwen 2016]

Although there are no products with such thin wafers commercially available today, it is assumed that with the current conditions and today's cost breakdown of the different components, a significant production capacity of such technology (e.g. 1GWp/year) would lead to those numbers.

The ultimate wafer costs have been assumed by observing the evolution of costs over the last years and by assessing the most influential parameters for the cost change. From this experience curve a percentage of further cost reduction has been assumed.

It has been recorded that wafer prices are mainly impacted by the silicon usage in combination with the price of silicon (USD/kg). The price of silicon has been subject to certain volatilities in the past such as supply and demand mismatches in 2008, expansion in new markets and redefined margins, however apart from some peaks the price has followed a rather stable learning curve where ranges of 13 – 25 USD/kg can be spotted. This has been documented by [Louwen 2016] and is in line with the

[6] Source: PVinsights and EnergyTrend

consortium's relevant experience. Figure 2 presents the development of the silicon price and the impact they have on the price of wafer.

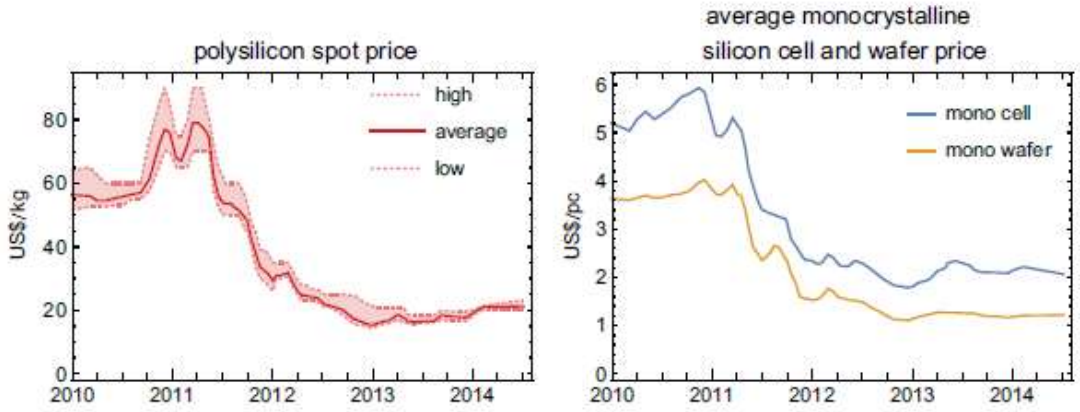

Figure 2: Overview of development of polysilicon prices (left graph) and wafer prices (right graph, brown curve) [Louwen 2016]

[Goodrich 2013] has also reported that besides the silicon use (wafer thickness) the sawing losses are also contributing to cost reduction for Si-wafers. Therefore the choice for sawing (slurry or diamond saw) and the thickness of wire for cutting will also contribute to further current cost reduction and yield improvement. Indicatively, for the wafering processing and the production yield process, the consortium has used the below in their estimations:

- For a 20kg and 200mm round ingot giving 156x156 pseudo-square substrates with around 95% yield
    - With 120µm wire the following is possible:

    Production of 180µm wafers with 0.41 USD/wafer and an amount of around 855 wafers
    Production of 120µm wafers with 0.33 USD/wafer and an amount of around 1069 wafers
    - Reducing the wire thickness from 120 µm to 80µm allows:

    Production of 120µm wafers with 0.27 USD/wafer and an amount of 1283 wafers

Regarding the epitaxial wafer costs, costs have been calculated with the use of IMEC's model. Today this technology is not commercially available and therefore there is no good reference to assume current costs. However, following the assumptions of chapter 4.1 the ultimate cost was calculated for a 156x156mm substrate of 40 um thickness. The model was run using different scenarios also for 125x125mm substrates and extrapolating the results to 156x156mm substrates. Results converged to an average value of 0.27 USD.

Table 1: Wafer Costs in USD ($) for 4 different substrate thicknesses. The standard substrate is the reference wafer of 180 µm. Current costs assumes average values of 2015. "Ultimate" wafer costs are defined as the estimated future prospective minimum costs.

Substrate	Standard 180µm	Thin 120µm	Ultra-thin 80µm	Epi-foil 40µm
Current wafer cost (COGS in USD/item)	0.9	0.76	0.67	n/a
Current wafer cost (COGS in USD cents/Watt)*	18.0	15.2	13.4	n/a
Ultimate wafer cost (COGS in USD/item)	0.66	0.55	0.49	0.27
Ultimate wafer cost (COGS in USD cents/Watt)*	13.2	11.0	9.8	5.3

**The tranlation from USD/item to USD/watt uses the information from [Louwen 2016] and assumes an IBC 60 cell module of 20.5 % efficiency and power output around 300 Wp, which has been defined as a benchmark. This equals 5 Wp per cell (wafer) with a cost of 0.9 USD for the case of standard 180µm. Therefore this leads to 0.18 USD/Wp. The same approach has been followed for the rest of the substrates.*

From the results of the above table it is already very clear that the cost impact of moving to thinner wafers in conjunction with improved wafering processes is significant, no matter the cost of polysilicon. Thicknesses of 80µm would be around 26% less than the standard substrates (both in current and ultimate scenario) while introducing epi-foils this cost reduction potential can increase to 59.8%.

That creates a very promising environment for commercialisation of those thin wafer based technologies in the coming years.

3.2. Impact on cell costs

Following on the calculation process to identify the impact on the cell cost, additional assumptions had to be made on top of the ones described in chapter 4.2. Those are the breakage rate (or the cell processing yield) and the cell processing cost, presented in Table 2 and Table 3.

The breakage rate for ultra-thin wafers is a good estimation based on preliminary results which rely on low consolidated volume that was used to estimate a mid-term optimized production breakage rate. It is a fact that the thinner the wafer the more difficult it becomes to handle and to process. This is especially noticeable for thicknesses below 100µm where the breakage rates increase. This of course is related to the availability of adequate equipment and manufacturing lines to treat properly these sensitive substrates. For the ultimate scenario it is assumed that such improved equipment will be in place.

Regarding the cell processing costs, it is considered rather constant for all substrates. The cell processing includes a standard treatment of the wafer (cleaning and texturing), diffusion, wet chemical treatment, the silver-based grid (metallization) and the deposition of TCO, with no significant changes assumed in the different steps of processing. This is part of the global "business as usual" assumption.

However, minor adaptations based on the cell processing yield have be made to reflect better the ultimate scenario.

Table 2: Wafer breakage rate for the calculation of Cell Costs in USD ($) for 4 different substrate thicknesses. The standard substrate is the commercially available reference wafer.

Substrate	Standard 180µm	Thin 120µm	Ultra-thin 80µm	Epi foil 40µm
Breakage rate	1%	1%	3%	5%
(cell processing yield)	(99%)	(99%)	(97%)	(95%)

The numbers for the cell processing do not include the cost of the wafer, therefore, for the total cost of cell those two needed to be added (see Figure 3).

Table 3: Cell Costs in USD ($) for 4 different substrate thicknesses. The standard substrate is the reference wafer. Current costs assume average values of 2015. "Ultimate" wafer and cell costs are defined as the estimated future prospective minimum costs

Substrate	Standard 180µm	Thin 120µm	Ultra-thin 80µm	Epi foil 40µm
Current wafer cost (COGS in USD cents/Watt)*	18.0	15.2	13.4	n/a
Ultimate wafer cost (COGS in USD cents/Watt)	13.2	11.0	9.8	5.3
Ultimate wafer cost corrected for yield (COGS in USD cents/Watt)**	13.2	11.0	10.0	5.6
Current cell processing cost (COGS in USD cents/Watt)*	15.0	15.0	15.0	n/a
Ultimate cell processing cost corrected for yield (COGS in USD cents/Watt)**	15.0	15.0	15.3	15.6

**The figure was derived from [Louwen 2016].*

***The figures have been adapted considering the yield efficiency assumed in Table 2.*

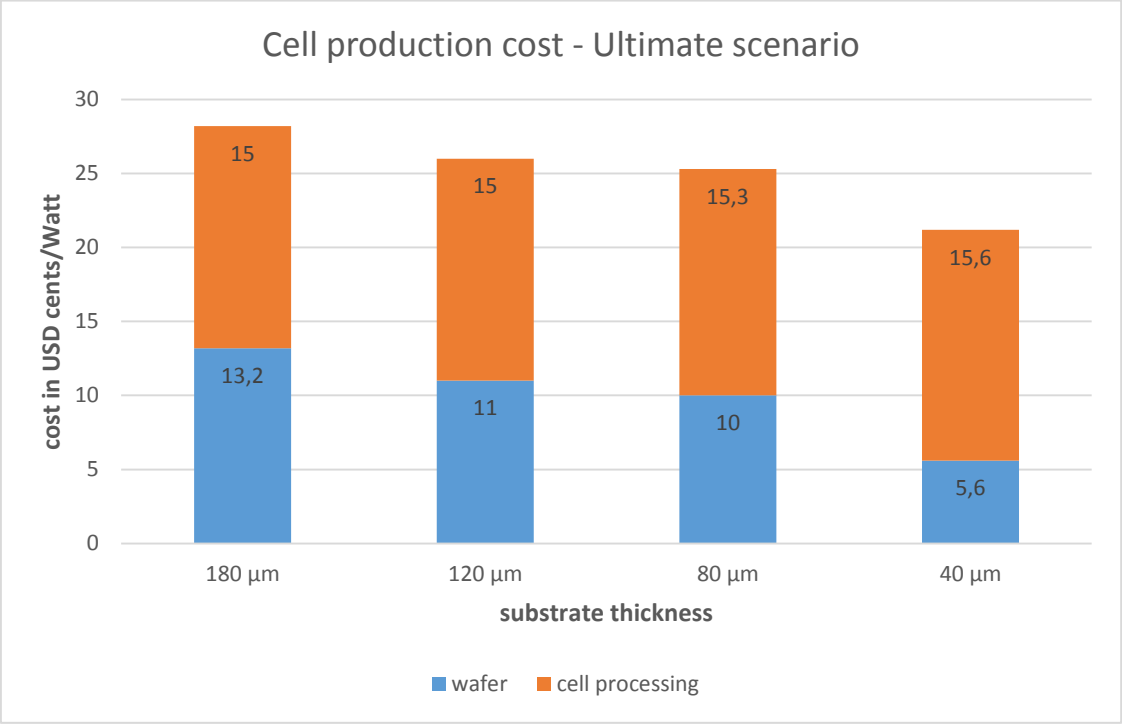

Figure 3: Cell production costs (COGS) for the ultimate scenario

Results from Table 3 and Figure 3 show a significant cost reduction at the cell level which reaches 35.8% when comparing epi-foil based cells with current cell technologies and 24.8% when comparing with projected costs for ultimate cell (180 µm) technologies.

As implied above the cell processing cost increases with lower thicknesses. This can be explained by the decrease of the total MW produced, due mainly to two factors: the increased breakage rate that we noticed above (Table 2) and the reduction in cell (and module) efficiency. However, in total the cell costs remain lower in thinner substrates.

At this point it should be noted that this analysis is limited to one cell type of technology i.e. heterojunction based cells (IBC-SHJ). However, one could grow an emitter and/or BSF/FSF[7] during the epi-foil growth *at no extra cost*, which could actually lead to a further cost reduction at cell level (compensating perhaps the effect of lower yield and efficiency) depending on the cell type that is used. Hence, it is not necessarily so that for an epi-foil the cell cost per Watt should be higher than for a regular thickness cell.

3.3. Impact on module costs

To calculate the cost of the module, the module development costs (or module elements production costs) needs to be added on top of the cell cost. Those elements include normally the cost of stringing/tabbing or other interconnection, the cost of the conductive adhesive, the EVA cost, the back sheet cost, the cost of frame, glass and junction box and other costs with different shares depending on the technology, but no real difference in terms of total cost [Louwen 2016].

[7] BSF: Back Surface Field, FSF: Front Surface Field

In order to create a benchmark for these costs, a module of 0.51 USD for a standard 180 µm substrate was assumed for current costs [Louwen 2016]. For 120 and 80 µm substrates lower wafer costs were taken into account as shown above, but keeping all other parameters and module efficiency constant and neglecting yield losses.

For the ultimate costs, a similar approach was chosen meaning that the ultimate wafer costs were now taken into account, keeping all other parameters and module efficiency constant and neglecting yield losses. An additional assumption that was implemented was a cost reduction of 0.01 USD from back sheet material.

Table 4: Module Costs in USD ($) for 4 different substrate thicknesses. The standard substrate is the reference wafer. Current costs assumes average values of 2015

Substrate	Standard 180µm	Thin 120µm	Ultra-thin 80µm	Epi foil 40µm
Current wafer cost (COGS in USD cents/Watt)	18.0	15.2	13.4	n/a
Ultimate wafer cost (COGS in USD cents/Watt)	13.2	11.0	9.8	5.4
Ultimate wafer cost corrected for yield (COGS in USD cents/Watt)	13.2	11.0	10.0	5.6
Current cell processing cost (COGS in USD cents/Watt)	15.0	15.0	15.0	n/a
Ultimate cell processing cost corrected for yield (COGS in USD cents/Watt)	15.0	15.0	15.3	15.6
Current integral module cost (COGS in USD cents/Watt)*	51.0	48.0	46.0	n/a
Ultimate integral module cost (COGS in USD cents/Watt)*	45.2	42.8	41.4	36.3

**Including wafer, cell processing and all other costs of module processing and materials*

The costs of modules have been corrected based on two factors: the module efficiency and the cell production yield. The correction for module efficiency assumes lower cell and module efficiencies for thinner wafers. Similarly the correction for cell yield assumes lower cell processing yield for thinner wafers.

These closer-to-reality corrected numbers as well as the assumed module efficiencies are presented in Table 5. The final set of numbers was used to calculate the module development costs (see Figure 4).

Table 5: Module Costs in USD ($) for 4 different substrate thicknesses corrected for module efficiency and cell production yield.

Substrate	Standard 180µm	Thin 120µm	Ultra-thin 80µm	Epi foil 40µm
Module efficiency (%)	20.5	20.5	20	19.5
Ultimate module cost corrected for module efficiency (COGS in USD cents/Watt)	45.2	42.8	42.4	38.2
Ultimate module cost corrected for module efficiency and cell yield (COGS in USD cents/Watt)	45.2	42.8	42.9	39.1

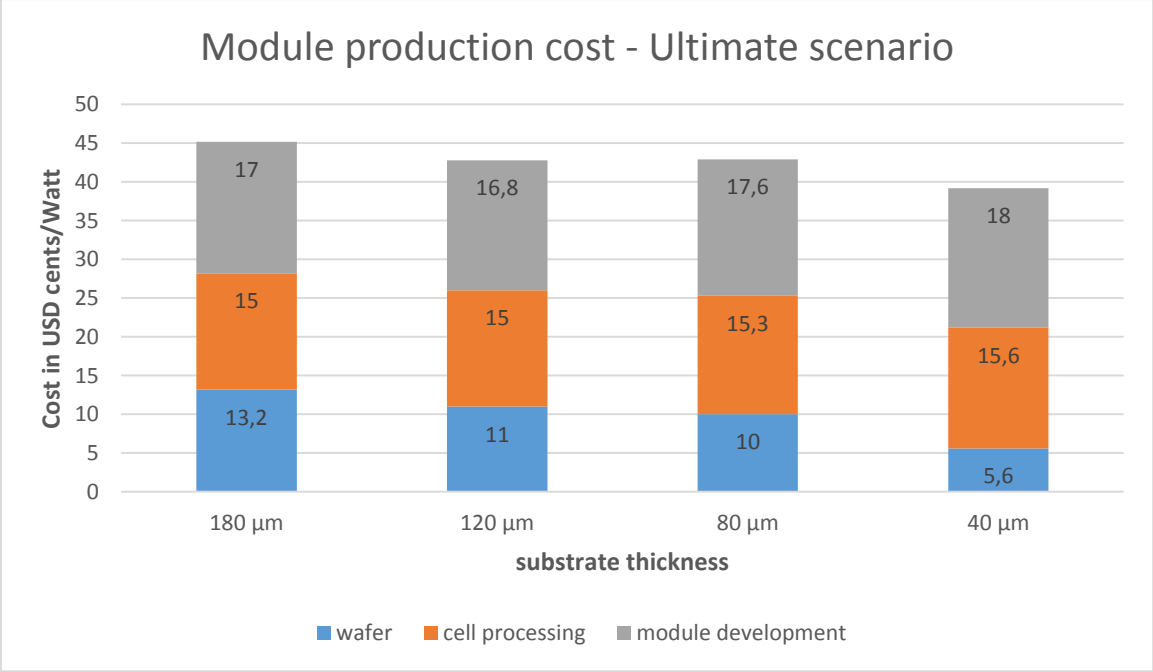

Figure 4: Module production costs (COGS) for the ultimate scenario – corrected values for module efficiency and cell yield were used to retrieve the module development share

From Tables 4 and 5 a cost reduction potential for the integral module costs of 23.4 % can be derived, taking 0.51 USD/Wp for the chosen benchmark compared to 0.391 USD/Wp for the ultimate module based on epi-foil wafers. If projected cost reductions for 180 µm wafers are taken into account the future benchmark costs would be at a level of 0.452 USD/Wp and the cost reduction potential would be 13.5 %.

Regarding the cost reduction potential for wafers 57.6% can be derived when comparing 0.056 USD/Wp for epi foil with 0.132 USD/Wp for "ultimate" wafers of 180 µm and 68.9% when comparing with benchmark cut wafers (0.18 USD).

Module assembly (process and materials) costs are dominated by materials which are standard and common for use in solar PV. Therefore the cost reduction potential is assumed low (typically 0.01 USD/Wp as mentioned earlier could be saved by alternative back sheet material) and not much more gain is expected.

3.4. Sensitivity analysis

Some of the main assumptions used in the above calculations for correcting cost values are the module efficiency and the yield, both of which are assumed to be lower for the epi-foil based module. Therefore, a simple sensitivity analysis has been made in order to identify the magnitude of the cost reduction changes when changing these parameters. This will illustrate the effect of our assumptions on the final cost and cost reduction and assess the impact of different scenarios/combinations, giving an indication of the boundaries beyond which the research community and industry should aim.

Module efficiency (%)

Production yield (%)	18,5	18,7	18,9	19,1	19,3	19,5	19,7	19,9	20,1	20,3	20,5	20,7	20,9	21,1	21,3	21,5
80	0,451	0,447	0,442	0,438	0,434	0,430	0,426	0,423	0,419	0,415	0,412	0,408	0,405	0,401	0,398	0,395
81	0,448	0,444	0,439	0,435	0,431	0,427	0,423	0,420	0,416	0,412	0,409	0,405	0,402	0,398	0,395	0,392
82	0,445	0,441	0,436	0,432	0,428	0,424	0,420	0,417	0,413	0,409	0,406	0,402	0,399	0,395	0,392	0,389
83	0,442	0,438	0,433	0,429	0,425	0,421	0,417	0,414	0,410	0,406	0,403	0,399	0,396	0,392	0,389	0,386
84	0,439	0,435	0,430	0,426	0,422	0,418	0,414	0,411	0,407	0,403	0,400	0,396	0,393	0,389	0,386	0,383
85	0,436	0,432	0,428	0,424	0,419	0,416	0,412	0,408	0,404	0,400	0,397	0,393	0,390	0,387	0,383	0,380
86	0,433	0,429	0,425	0,421	0,417	0,413	0,409	0,405	0,401	0,398	0,394	0,391	0,387	0,384	0,380	0,377
87	0,431	0,426	0,422	0,418	0,414	0,410	0,406	0,402	0,399	0,395	0,391	0,388	0,385	0,381	0,378	0,375
88	0,428	0,424	0,420	0,415	0,411	0,407	0,404	0,400	0,396	0,392	0,389	0,385	0,382	0,378	0,375	0,372
89	0,426	0,421	0,417	0,413	0,409	0,405	0,401	0,397	0,393	0,390	0,386	0,383	0,379	0,376	0,373	0,369
90	0,423	0,419	0,415	0,410	0,406	0,402	0,398	0,395	0,391	0,387	0,384	0,380	0,377	0,373	0,370	0,367
91	0,421	0,416	0,412	0,408	0,404	0,400	0,396	0,392	0,389	0,385	0,381	0,378	0,374	0,371	0,368	0,364
92	0,418	0,414	0,410	0,406	0,401	0,398	0,394	0,390	0,386	0,382	0,379	0,375	0,372	0,369	0,365	0,362
93	0,416	0,412	0,407	0,403	0,399	0,395	0,391	0,387	0,384	0,380	0,377	0,373	0,370	0,366	0,363	0,360
94	0,414	0,409	0,405	0,401	0,397	0,393	0,389	0,385	0,381	0,378	0,374	0,371	0,367	0,364	0,361	0,357
95	0,411	0,407	0,403	0,399	0,395	0,391	0,387	0,383	0,379	0,376	0,372	0,368	0,365	0,362	0,358	0,355
96	0,409	0,405	0,401	0,396	0,392	0,388	0,385	0,381	0,377	0,373	0,370	0,366	0,363	0,359	0,356	0,353
97	0,407	0,403	0,398	0,394	0,390	0,386	0,382	0,379	0,375	0,371	0,368	0,364	0,361	0,357	0,354	0,351
98	0,405	0,400	0,396	0,392	0,388	0,384	0,380	0,376	0,373	0,369	0,365	0,362	0,359	0,355	0,352	0,349
99	0,403	0,398	0,394	0,390	0,386	0,382	0,378	0,374	0,371	0,367	0,363	0,360	0,356	0,353	0,350	0,346

Figure 5: Sensitivity analysis for assessing the different impact of module efficiency and production yield on epi-foil based module costs

The green areas in the graph show which one should be the combination of module efficiency and production yield in order to provide a product (module) at a cost lower than the cost of the ultimate standard module (0.452 USD/W). *What is seen in Figure 5 is that with the production yield and module efficiency range chosen there is no scenario/combination that will lead to a more expensive epi-foil module than the ultimate reference 180µm module*. The yellow part of the figure reflects the scenarios where the epi-foil module will reach values above our result (0.391 USD/W) but lower than the standards product while the green areas are the scenarios where costs could decrease further. What is promising to see is that even in worst case scenarios (80% production yield and 18.5% module efficiency) the final product (epi-foil) is cheaper.

4. Conclusions and future work

The current report provides a reality check on the cost impact of the research innovations brought by the Cheetah project in the field of wafer-based c-Si PV technologies. More specifically a step-by-step calculation approach was followed in order to assess the cost impact of the use of ultrathin and epitaxial wafers instead of conventional 180 um thick wire-sawn wafers.

Besides all the different technical challenges (e.g. more complex cell processing) and supply chain uncertainties it was shown that the work of Cheetah is very promising and deserves further investigation. Our calculations show that there is ***a 23.4% cost reduction potential on module level when replacing standard wire-sawn wafers with ultra-thin epitaxial foils in the chosen SHJ-IBC cell and module technology.*** This fulfils one of the KPIs of the project (KPI 8.2) which aims for 20% cost reduction comparing to state of the art technologies at the beginning of the project (2014).

The results showed that comparing ***epi-foil based modules to standard products*** (i.e. 180 µm wafer based) considering their future prospective cost reduction potential (due to cheaper polysilicon and/or improved processes)***, savings of 13.5% can be achieved***. This reveals the competitiveness of the technology under development based on thin wafers.

Regarding the cost reduction potential on ***epi-wafers*** this is found to be very impressive at a level of ***57.6% when comparing with projected costs for "ultimate" wafers (180 µm)*** and of ***68.9% when comparing with benchmark cut wafers (180 µm)***. Both exceed by far the defined KPI of Cheetah project which was set for 30% (KPI 6.5).

For the ultra-thin cut wafer (80µm) modules and the thin cut wafer (120µm) modules the results were very promising too. The cost reduction potential for the ***ultra-thin technologies was calculated 15.8% when comparing with benchmark modules and more than 5% when considering the ultimate scenario for the standard module.*** Similarly, for the ***thin wafer based modules (120µm substrate)*** the results were of the same scale – slightly more positive i.e. ***16.1% and 5.3% respectively***. The reason is, as mentioned, the combination of lower yield and module efficiency in thinner substrates – more obvious below 100µm.

Wafer costs for thicknesses of 80µm would be around 26% less than the standard substrates (both in current and ultimate scenario) while for 120µm the cost reduction reaches 16.7%.

A future version (final report, end of 2017) will attempt to provide a more detailed study on the cost impact of wafer handling and cell processing incorporating additional expertise from the research community as well as from the industry sector. Any future feedback received on this report upon publication will be evaluated. In addition, future work will include the assessment of the research work on advanced light management for thin-film PV (TF) and on Organic PV (OPV) in accordance with the EERA-PV objectives.